Reconfigurable Self-timed Elements

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November 29, 1996

Abstract

The proposed presentation is in two parts. The first part briefly outlines my research into self-timed FPGA architectures, in particular FPGA architectures with SRAM configuration memories. A property of SRAM FPGAs is that they are in-system reconfigurable; this property is being used in a new class of system known as *transformable* or *virtual hardware* systems. However exploiting the reconfigurability of SRAM FPGAs is difficult since the reconfiguration software must always be conscious of the delays within the FPGA. By using a self-timed FPGA architecture, configuration software can be freed from needing to reason about these delays, thus allowing the reconfigurability to be exploited more easily, and potentially on-the-fly.

The second part of the presentation, highlights one area of my work is that of more general interest to asynchronous research community: reconfigurable self-timed elements. These elements are generalisations of standard self-timed element for synchronisation (*the reconfigurable C-Muller gate*), and for control (*the Select/Q-Merge pair*). The reconfigurable C-Muller gate allows an arbitrary synchronisation pattern to be defined between a set of inputs. It has application beyond FPGAs to general routing applications.

The Select/Q-Merge pair allows a wide variety of control structures to be implemented, including variants of all the control blocks used by Sutherland in his Micropipeline paper. An important aspect of the Select/Q-Merge pair is their symmetry in definition and usage, which matches well with the symmetry that Sutherland highlights in the use of C-Muller gates in Micropipelines.

Finally, the presentation briefly discusses how these synchronisation and control elements can be integrated together with delay elements to form a reconfigurable timing cell. These timing cells are used in the author's work on the STACC self-timed FPGA architecture.

1 Introduction

The rest of this summary is structured in a similar way to the slides intended for presentation. Where further explanation is required to the bulleted points for the slides, this is indicated by the use of comments in square brackets.

2 Slides

2.1 FPGAs

- FPGAs:
  - similar to MPGAs [Mask Programmable Gate Arrays]
  - configured differently

- Configuration Memory:
  - Fuse-based
  - SRAM-based: in-system reconfigurable
- SRAM FPGAs: 'soft-hardware'
  - Software Like: load and run configuration like program
  - Hardware Like: signal delay problems
- Reconfigurability exploited in *virtual hardware systems*

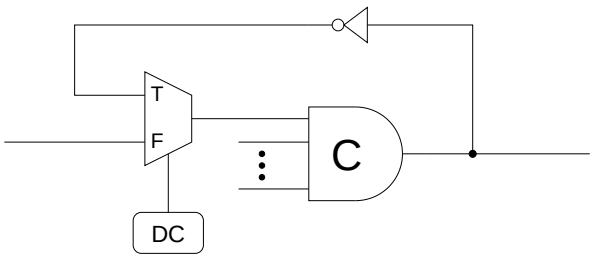
2.2 Self-Timed FPGAs

- For prototyping:
  - MONTAGE: U.Washington
  - PGA-STC: U.C.Davis
- For Virtual Hardware
  - STACC: Edinburgh
- STACC:
  - dedicated bundled data protocol
  - clean split between data and control arrays

2.3 Self-timed Elements

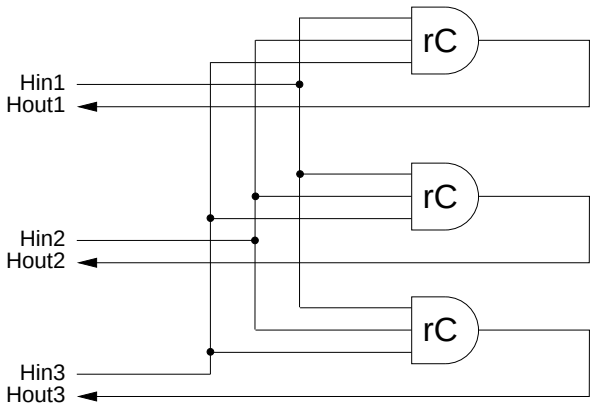
- Self-timed Elements
  - Synchronisation (C-Muller gates)
  - Control (Select,Merge,Toggle,Call,etc.)
  - Delay (Data-Bundling, Isochronic forks)
- Reconfigurable Elements
  - require a few , ideally one, flexible element

2.4 Synchronisation Elements



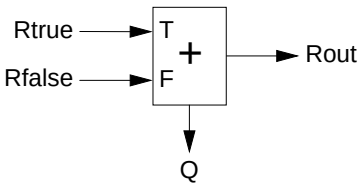
- Reconfigurable C-Muller Gate
  - `DC` determines whether each input is involved in synchronisation
  - implement any fixed pattern of synchronisation
  - small number of configuration bits

2.5 Reconfigurable C-Muller Cross-bars

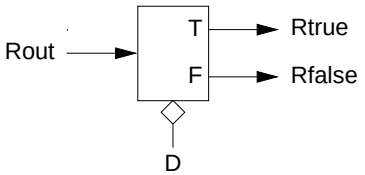


- several reconfigurable C-Muller gate with common input signals
- operates on handshaking pairs
- can synchronise arbitrary data flow pattern: i.e. cross-bar switch
- applications: routing
  - e.g. self-timed FPIDs [Field Programmable Interconnect Devices]

2.6 Select and Q-Merge



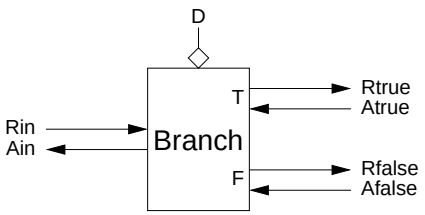
Q-Merge

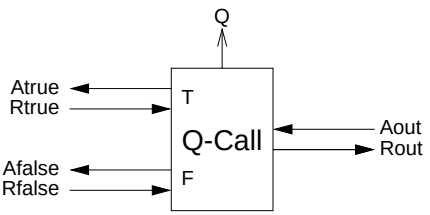


Select

- Symmetry:
  - Select: bundled-data to dual-rail
  - Q-Merge: dual rail to bundled-data
- can be defined in two-phase or four-phase
- Q-Merge can include arbitration
- Select / Q-Merge Pair is a good building block for control elements [see following slides]

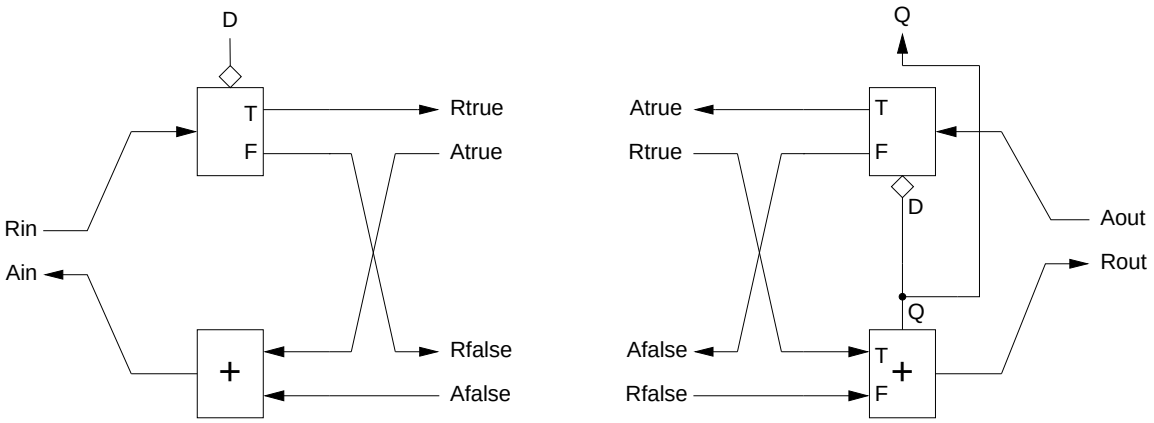
2.7 Q-Call and Branch





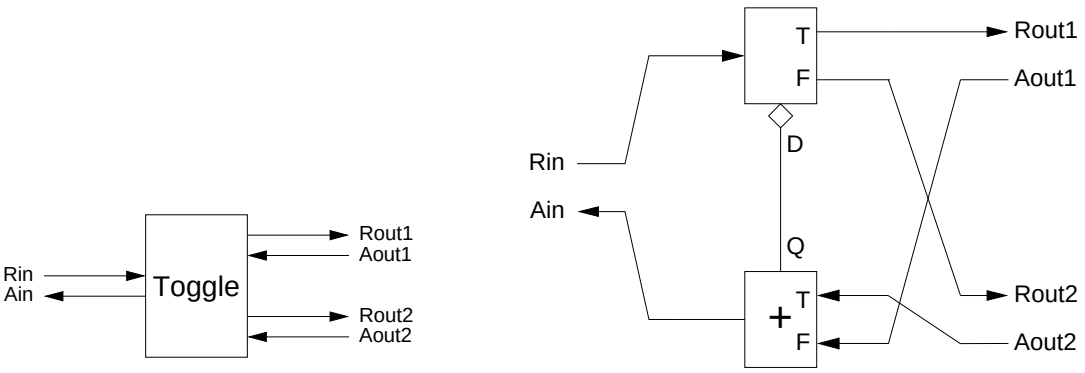
- Operate on Handshaking Pairs
- Again Symmetrical
- Q output indicates last call request to be granted
- construct using Select/Q-Merge pair [Next Slide]

2.8 Use of Select/Q-Merge Pairs



Branch Q-Call

2.9 Toggled Branch



- Similar to Sutherland's Toggle, except operates on Handshaking Pairs

2.10 An Integrated Timing Cell

- Delay Elements
  - Fixed Delay
  - Variable Delay (e.g. CSCD)
- STACC Timing Cell
  - Integrates synchronisation, control and delay elements
  - Generates register control signals for localised self-timed region of FPGA

2.11 Summary

- Self-Timing is ideally suited to a reconfigurable environment such as FPGAs, since it accommodates variability in delays
- Reconfigurable C-Muller Gate
  - simple but powerful reconfigurable building block especially for routing
- Select and Q-Merge:
  - can implement variants of all modules used by Sutherland
  - good choice for standard library elements
- STACC:
  - integrates control functions in Timing Cell
  - general architectural model applicable beyond FPGAs