An open question - Will the properties of electromigration and thermomigration have an adverse effect on the future of asynchronous logic design?

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Abstract

The question is asked whether or not Electromigration and/or Thermomigration, phenomena that are both well known to cause the degredation of the physical structure of electronic circuits, will have serious consequences for the future research, development and application of asynchronous logic devices.

A non-rigorous answer to this question is presented that describes how the nature of asynchronous design, which in only performing useful work when processing actions dictate, will have the effect of causing temperature discontinuities to arise in that logic. This is precisely a factor that increases the rate at which electromigration and thermomigration effects are known to occur and therefore must have serious implications for the lifetime operability of asynchronous devices as opposed to equivalent synchronous machines.

A comparison is made between two hypothetical processors, one synchronous the other asynchronous, in order to support this argument.

1 Introduction

Electromigration and Thermomigration are phenomena that are well known to have adverse effects on the atomic structure of materials. In this paper these phenomena are examined with respect to electronic devices with particular emphasis being placed on the changes to the physical structure that may become manifest within asynchronous logic circuits.

Any asynchronous circuit has the potential to operate within a wide range of operational environments, for example within widely varying temperature gradients and non-constant voltage supplies. As these factors are precisely the circumstances in which electromigration, *EM*, and thermomigration, *TM*, effects become prominent, the question is asked whether or not asynchronous logic design will ultimately be limited in scope and useability as compared to equivalent synchronous devices. This question becomes relevant when considered against the current drive towards the greater minaturisation of electronic devices especially as those devices will be likely to employ a greater current density flow which itself in turn increases *EM* and *TM* effects.

2 Electromigration

Electromigration is a well documented transport phenomena that is known to occur within solids. Essentially *EM* can be described as follows; In any electric field ions are subjected to a force due to that field and to a force which results from the motions of electrical carriers (electrons or holes). In bulk samples of solids (at very high temperatures, see section 3) these forces will cause the displacement of atoms by means of a lattice mechanism which results in the diffusion of atoms across a material. When considering thin films, *EM* is known to occur at much lower tempertures (but at higher current densities) by a grain boundary diffusion mechanism. *EM* will also cause failures at material discontinuities such as at terminals, temperature gradients and at structural inhomogenities. In general failure times due to *EM* are a function of;

- the activation energy for diffusion
- the exponents of the current density

As transistor sizes of 0.1 micron and less are now being proposed there is the situation that as the dopants in such circuits are of such small quantities any alteration to the average distribution of those dopants will have a significant effect on the circuit performance.

In the invertor circuit in figure 6 below we can see that when there is a change from the $1 \rightarrow 0$ state or the $0 \rightarrow 1$ state there is **uni-directional** flow of current through the transistors of that circuit. It is this uni-directional aspect of current flow that has a net result of there being *EM* and *TM* activity that will physically occur in those invertor transistors. This is a phenomenon that occurs in all electronic circuits.

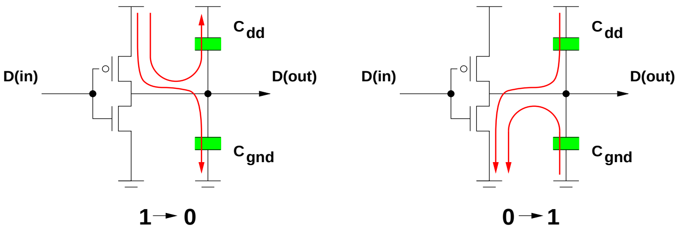

Figure 1: Uni-directional current flow through the transistors of an invertor circuit.

3 Thermomigration

Thermomigration is defined as *"the flux of mass induced by a temperature gradient"* . Any electron, that has a temperature higher than the region into which that electron enters, will be diffused towards a cooler region almost as if a potential were acting upon that body. This *thermodynamic potential* gives rise to a thermodynamic force which is effectively a drift motion that is limited by the collisions of the electrons with obstacles.

If two regions in contact with each other are maintained at different temperatures mass transport can be observed to occur between those regions. In figure 2 we can see how if a portion of a conductor is maintained at a higher temperature than the rest of that conductor, thermomigration effects will cause depletition of ions in the hot zone with corresponding ion accumulation downstream in the direction of the carrier motion;

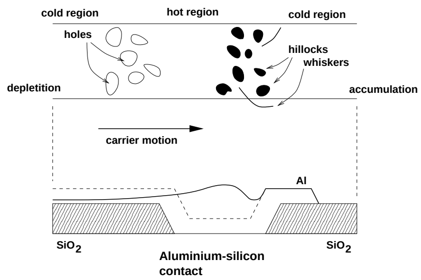

Figure 2: Temperature gradients across a conductor.

4 The problem with asynchronous logic?

There are many reasons why designers are now proposing that asynchronous logic is the next step forward in digital circuit design but for the purpose of this discussion we are only interested in the following main argument:

- **low power:** A typical synchronous circuit, will employ a global clock which means that the majority of that circuit will be active at all times. The continual decrease in CMOS process rules has meant that modern CMOS logic has become much denser and faster to the point where modern microprocessors can be expected to dissipate 20 to 30 watts of power. With the current trend towards even greater minaturisation these problems of power dissipation will continue to increase. The lack of a clock in an asynchronous circuit means that only those parts of the logic that are requested to perform any processing actions will be powered. Asynchronous logic design therefore tends to be inherentely "low powered" in aspect.

In the first instance let us consider two microprocessor circuits, both of which are designed to be equivalent devices, one of these structures is synchronous with the other device being asynchronous. Let us now consider two cases of operational environments for our two processors. The first case will involve constant ambient temperature and power supply whilst the second will involve both changing ambient temperature and power supplies.

4.1 Constant temperature and current supply

Before we require our circuits to perform any processing actions we wait a period of time for both devices to reach their operational temperatures which we can see below if we look at the two temperature maps of the surface area, figure 3.

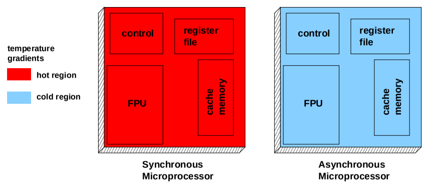

Figure 3: Operational temperatures of both processors.

Immediately we can see that the temperature of the two processors is not the same. The synchronous device will likely operate at a much higher temperature due to the fact that the synchronous clock will be continually in operation even though no useful actions are being performed (the clock is continually active in our example). We then request our devices to carry out the execution of a task, which does not require the use of the FPU unit, and then after a period of time we again look at the temperature of the surface area of our devices, figure 4;

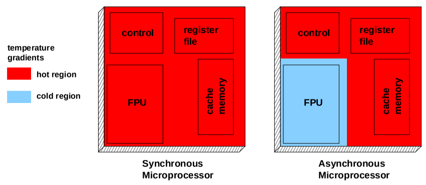

Figure 4: Temperatures of both processors after a period of sustained work.

We can now see how an asynchronous circuit is implicitly low powered as only those areas of the processor that are active will be powered and this is shown by the differing temperature regions across the surface of the device. Note that the synchronous processor is unlikely to have significant temperature changes after processing due to the fact again that the clock signal will ensure that enough transitions will occur to keep the temperature constant.

Both processors are now given different tasks to do. These tasks involve the use of the FPU but only to the extent of about one in ten instructions actually use that unit. If we then re-examine the temperature maps of our devices we again see how there is a constant temperature gradient within the asynchronous unit across which useful work is actually being performed. The overall temperature of the FPU does not increase significantly as there is not a sustained period of activity in this area.

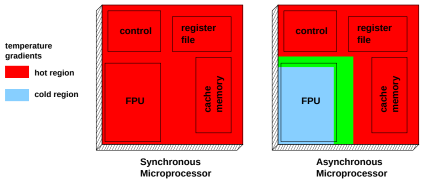

Figure 5: Temperatures of both processors after a period of sustained work involving the FPU.

This is the point where we see the percieved problem with asynchronous devices with regards towards *EM* and *TM* effects. At the temperature gradient near the FPU there will be significant thermomigration effects that will be observed in the logic that bounds that area. These problems do not occur within the synchronous device and as *EM* and *TM* can significantly reduce the MTBF figure of a circuit the conclusion must be drawn that if we are considering the overall lifetime of both our asynchronous and synchronous devices intuitively the lifetime of the asynchronous device must be less than that of the synchronous circuit. This problem can be summarised in the following hypothesis;

Hypothesis 1 *An asynchronous circuit that operates in an environment that has both a constant temperature and voltage power supply will have regions of circuitry across that device that will have differing temperatures. The boundaries between these regions will see enhanced electromigration and thermomigration effects take place that will significantly decrease the functional lifetime of that device.*

4.2 Variable temperature and current supply

In this environment both processors will be expected to operate under conditions of fluctuating temperature changes and variable power supplies, in essence any situation under which the operational working specifications of a device are exceeded.

When considering many of the modern synchronous microprocessor devices that are fabricated today we see that the working environmental specifications of these designs tend to be within narrow margins of operability, for example the Intel Pentium Processor (60/66 MHz model) has a working case temperature of 85^oC that is designed to restrict the surrounding ambient air temperature to a range of 40-45^oC. Typical voltage requirements of these devices are within the range of 3.3V $\pm$ 0.2V. The previous values are typical of the constraints that modern synchronous devices are expected to operate under but it is to be noted that this does not compare very favourably to asynchronous devices that have been demonstrated to have much wider tolerances to changes in operational conditions. The TITAC processor for instance, has an operational voltage of 5V but has been tested to work without error over a range of 2.5 to 7V. This is an order of magnitude greater of an operational constraint value.

Consider the following situation: Our asynchronous device, designed to work at say 3V, may be affected by an irregular power supply. This power supply may vary by several volts over time and so it must be that case that the device will experience greater temperature changes across the complete circuit due to the different rates of current density supplied. This of course will have a much greater impact when electromigration and thermomigration effects are considered as extreme temperature changes will enhance that rate at which such *EM* and *TM* effects occur. On the other hand our synchronous device, also designed to operate at 3V, when faced with a 5 or a 6V supply, may cease to function altogether. The point of this argument is to state that under fluctuating operational conditions the asynchronous device will be likely to continue functioning whilst the synchronous device may not. This leads us to our second hypothesis;

Hypothesis 2 *An asynchronous circuit may be best suited to operate in an environment that has both a fluctuating temperature and voltage power supply. The operation of such a device under such conditions will be likely to cause that circuit to have regions across that device that will have large differing temperatures. The boundaries between these regions will see greatly enhanced electromigration and thermomigration effects take place that will significantly decrease the functional lifetime of that device.*

4.3 How significant will these EM and TM effects really be?

The next question to be asked is whether or not these *EM* and *TM* effects are really likely to be a significant factor when considering the lifetime of any digital circuit be that device synchronous or asynchronous. Under normal working conditions we would expect our synchronous processor to have the longest operational lifetime whereas in abnormal working conditions the asynchronous processor may prove to have the longest life. But will this actually be the case? The biggest factor which may override any such effects will be due to the actual process of manufacture of such devices. It may be the case that such factors as:

- lack of temperature uniformity during film deposition
- non-uniform doping
- introduction of impurities

and other such aspects may have the overall effect that the actual working lifetime of such devices may be significantly below the time period that must elapse before *EM* and *TM* effects will become significant.

The conclusions that would have to be drawn that if the projected operational lifetimes of both our asynchronous and synchronous processors were the same then the asynchronous device would have to be employed as the processor of choice due to all the advantages of being low powered, tolerant to environmental conditions etc. We could assume that the problems related to *EM* and *TM* would never become significant issues where device lifetimes were to be considered and in cases where such devices were to be employed in hostile environments it may be that only the asynchronous devices would function correctly anyway.

5 Conclusions

We have seen intutively how asynchronous circuits must suffer from electromigration and thermomigration effects to a greater degree than equivalent synchronous devices up to the extent that the lifetimes of such asynchronous circuits may be significantly reduced. It may be that case that such effects will never be significant when considered against all the other factors that determine the physical lifetimes of such devices. Asynchronous logic design is still an important field of VLSI and microelectronic research and it is true that such logic has many specific roles to play with regards to specific types of operational environment.

Further research and modeling of *EM* and *TM* aspects must be carried out in order to determine whether or not these problems are likely to have such a specific impact on the useability and general future of asynchronous logic design.

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