Programme

Monday 2 July, 2001

1300 Registration

1330 Bundled-Data vs Clocked ASIC Design: ChipA - A Case Study
S.W. Moore, G.S. Taylor, R.D. Mullins and P. Robinson (Univ. of Cambridge)
1400 A Robust Asynchronous Communication System
Z.C. Yu and S.B. Furber (Univ. of Manchester)
1430 Yet Another Circuit Synthesis Method from Petri Nets
D. Furey (South Bank Univ.)
1500 Asynchronous Fault-Tolerant Biologically-Inspired Hardware
A.H. Jackson and A.M. Tyrell (Univ. of York)

1530 Coffee

1600 FSM Register Switching Activity Minimization for Low Power
I. Lemberski (South Bank Univ.)
1630 An Asynchronous ARM Compatible MMU Design and Implementation
F.T. Weigel and J.D. Garside (Univ. of Manchester)
1700 One-of-Four DI Codes in Technology Independent Synthesis
W.B. Toms (Univ. of Manchester)

1730 Presentations by attendees
1800 Business meeting

2000 Dinner - *Chinese Home Cooking Restaurant*, 34 West Preston St.

Tuesday 3 July, 2001

0900 Bridging Two Clock-Independent DTL IP Cores Via Asynchronous Pausible Clock Scheme
J. Xu (South Bank Univ.)
0930 Debugging Tools for Asynchronous Design
L. Janin and D.A. Edwards (Univ. of Manchester)
1000 Visualisation of Partial Order Models in VLSI Design Flow
A. Bystrov, A. Yakovlev and M. Koutny (Univ. of Newcastle)
1030 A Design Framework for Asynchronous Multithreaded Architectures
D.K. Arvind, J. Hossell, A. Koppe, T. Lewis, R. Rangaswami, J. Schneiders,
A. Stanley and S. Zhong (Univ. of Edinburgh)

1100 Coffee

1130 Extending the TK Model
A. Clarke and G. Stoyle (Univ. of Leeds)
1200 Split-Datapath Execution for Low Power
M. Evans (Univ. of Manchester)
1230 Analysis of Logic Gate Q-Flop Resolver
O. Maevsky, A. Bystrov, D.J. Kinniment and A. Yakovlev(Univ. of Newcastle)

1300 Close