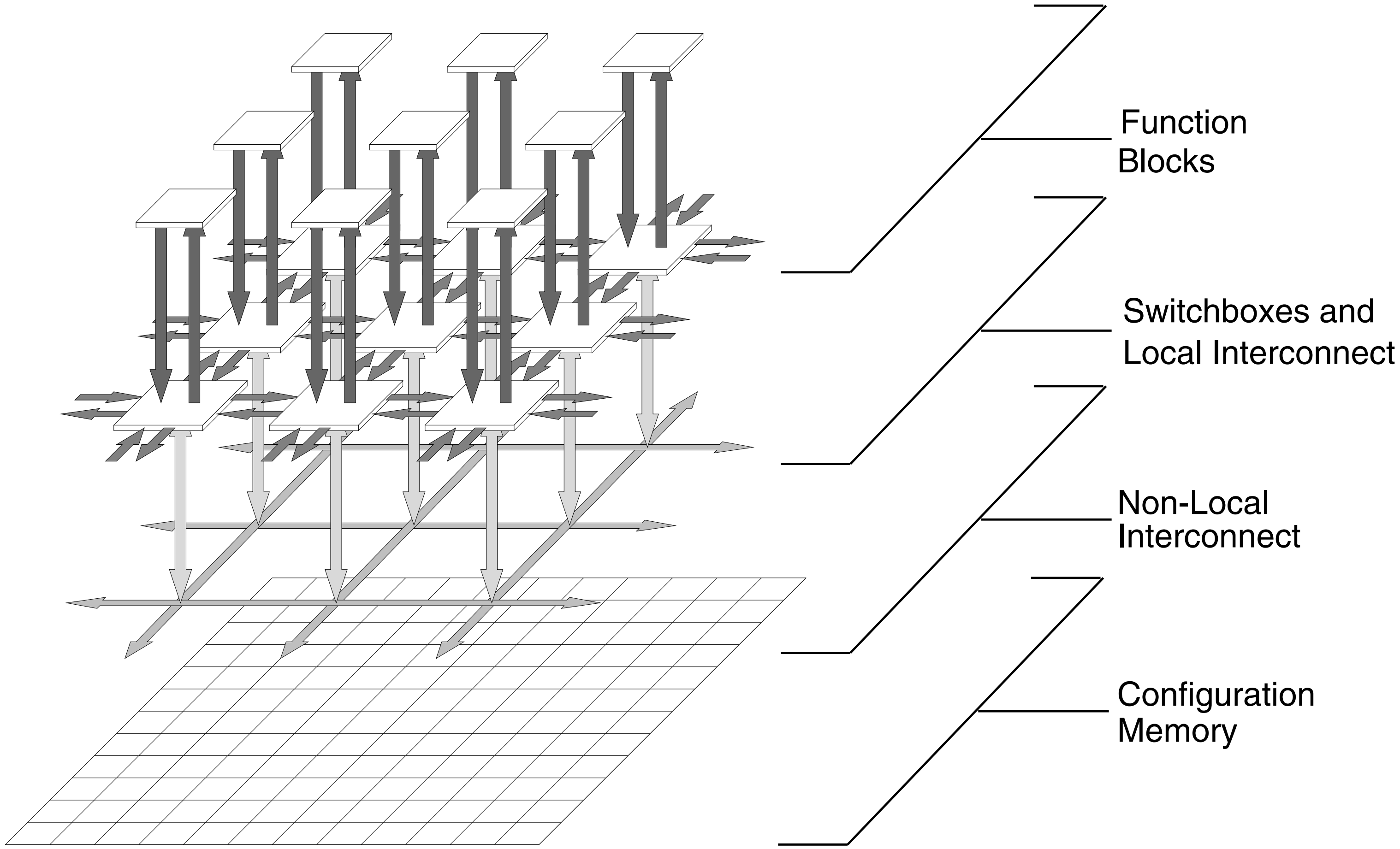
Self-Timed Reconfigurable Elements

Rob Payne

18th December 1996

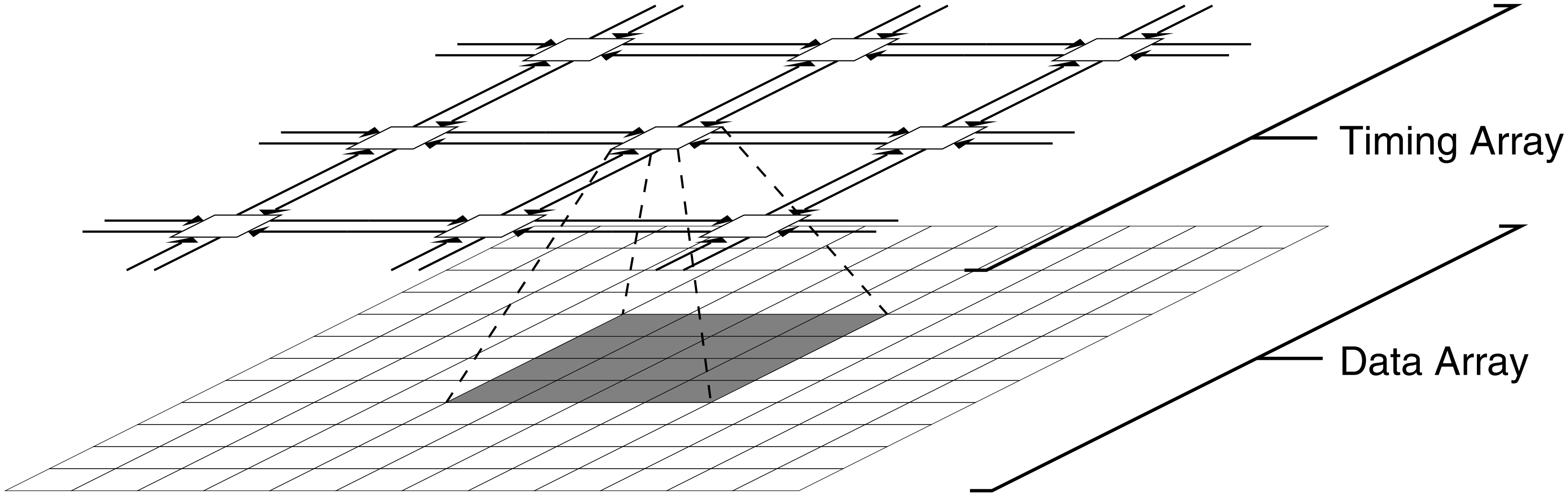

Function
Blocks
Switchboxes and
Local Interconnect
Non-Local
Interconnect
Configuration
Memory

FPGAs, Virtual Hardware and Self-Timing

- Configuration Memory: Fuse or SRAM based
- SRAM FPGAs: 'Soft-Hardware'
  - Software-like: load and run configuration like program
  - Hardware-like: routing/placement/partition all effect signal delay
- Reconfigurability on-the-fly exploited in *virtual hardware systems*
- Self-timing suits FPGAs, especially virtual hardware, since accommodates variability in delays.

Self-Timed FPGAs

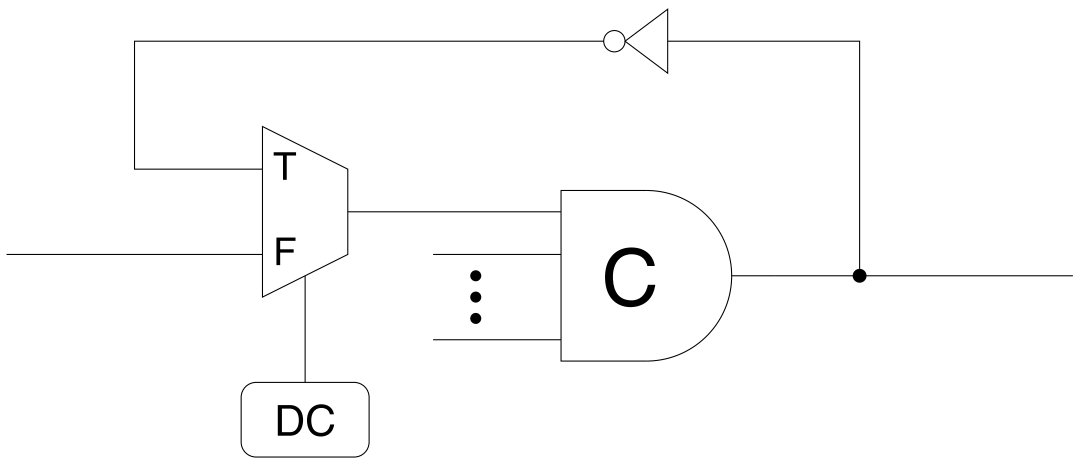
- For Prototyping:
  - MONTAGE: U.Washington
  - PGA-STC: U.C.Davis
- For Virtual Hardware
  - STACC: Edinburgh
- STACC:
  - dedicated towards bundled data implementations
  - clean split between data and control arrays
  - applicability beyond FPGAs



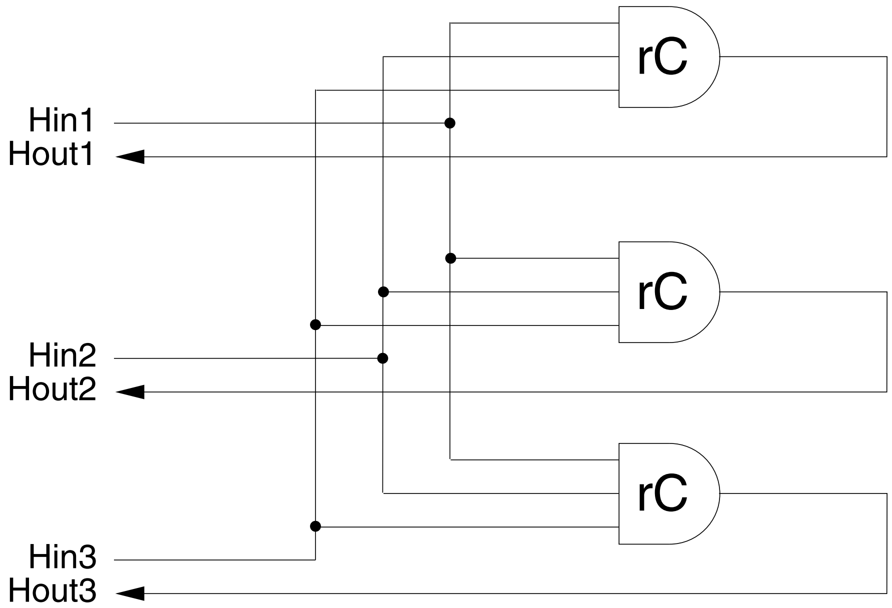
- Timing cells generate register control signals (local clocks) for localised region of FPGA

- Timing cells communicate via handshaking pairs

Reconfigurable C-Muller Gate

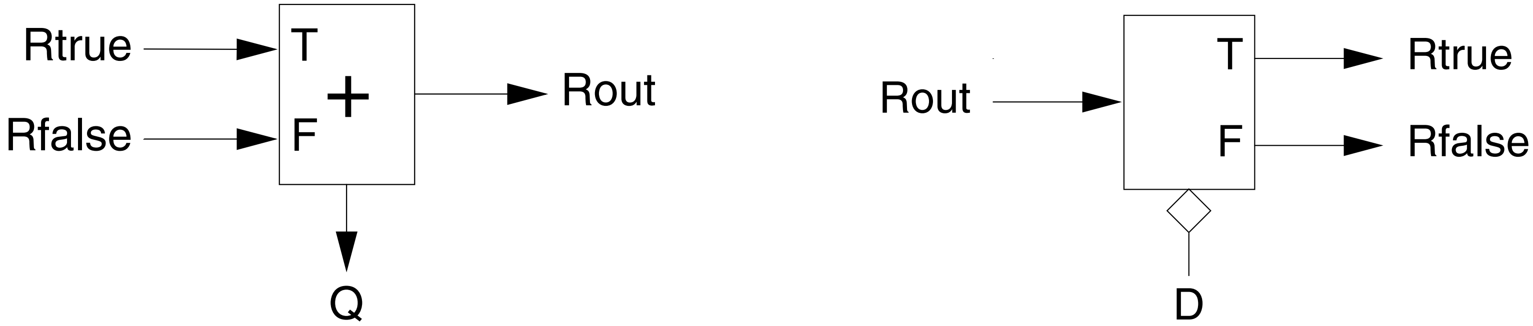


- `DC` determines whether each input is involved in synchronisation
- implement any fixed pattern of synchronisation
- small number of configuration bits: one per input



- reconfigurable C-Muller gates with common input signals
- synchronise arbitrary data-flow: i.e. cross-bar switch
- routing applications: FPIDs (Field Programmable Interconnect Devices)

Select and Q-Merge

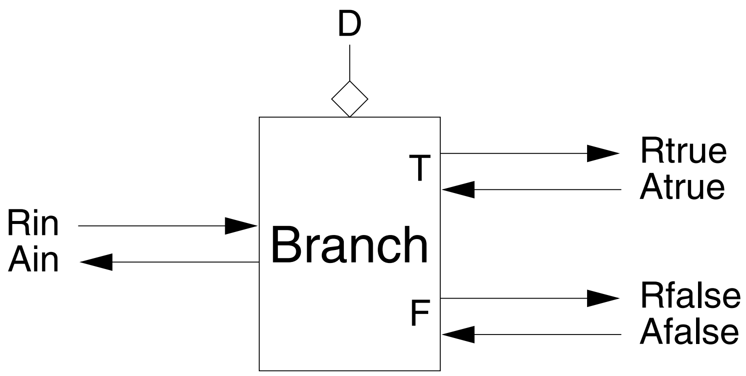


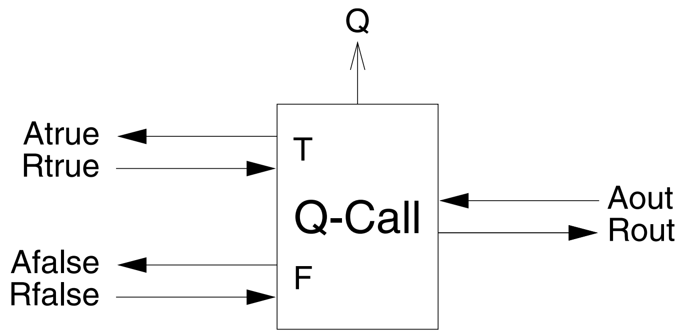
- Symmetry:
  - Select: bundled-data to dual-rail
  - Q-Merge: dual rail to bundled-data

- can be defined in two-phase or four-phase

- Q-Merge can include arbitration

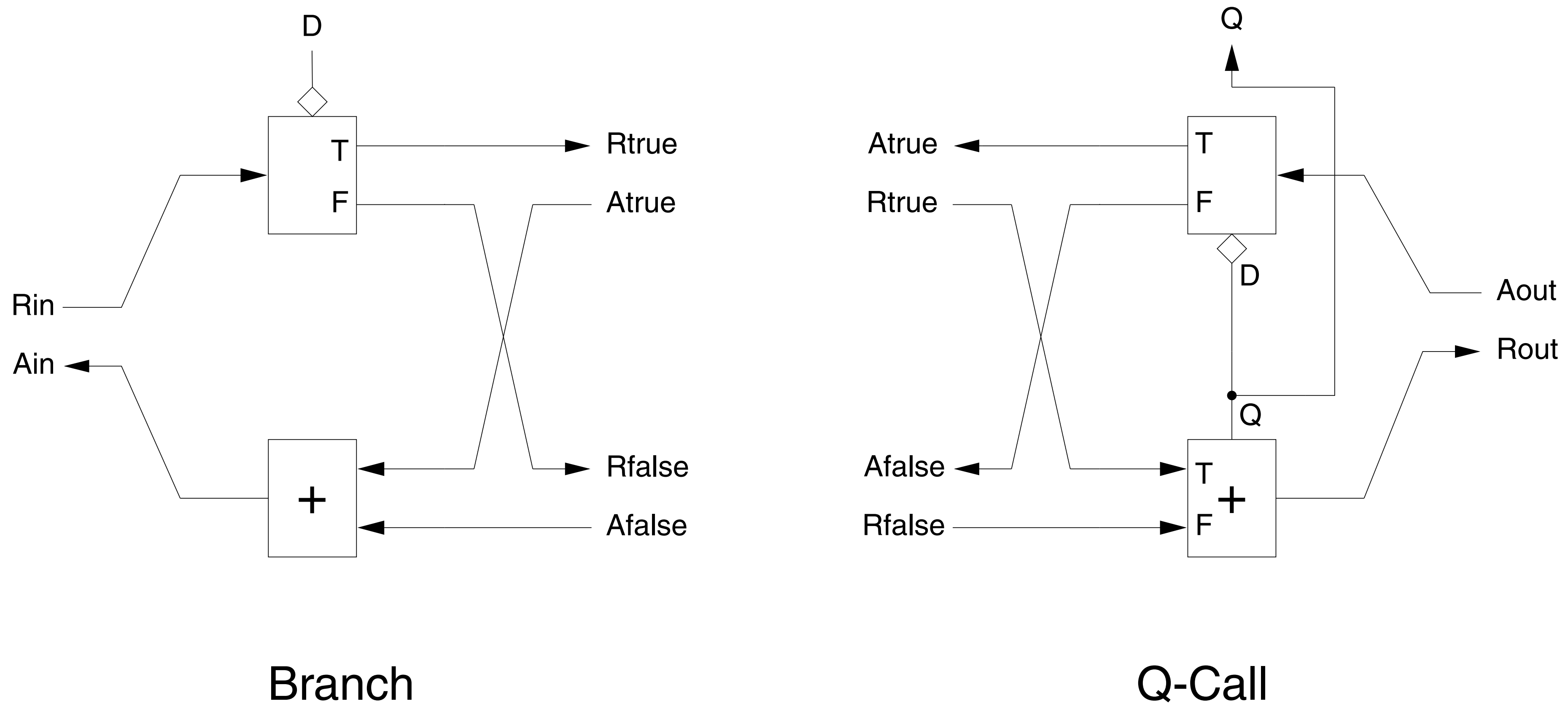
Q-Call and Branch



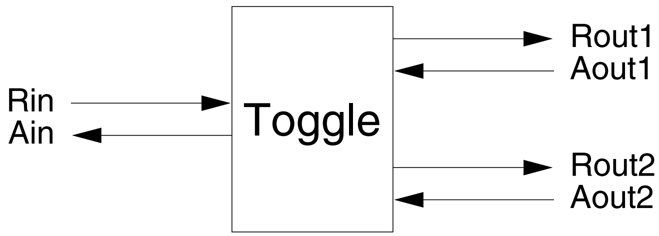


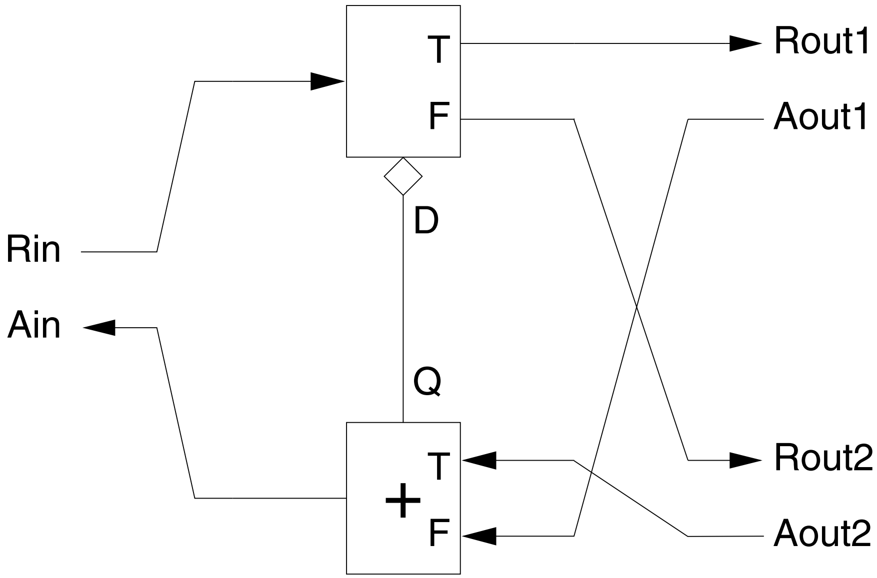
- Operate on Handshaking Pairs
- Again Symmetrical
- Q output indicates last call request to be granted

Use of Select/Q-Merge Pairs

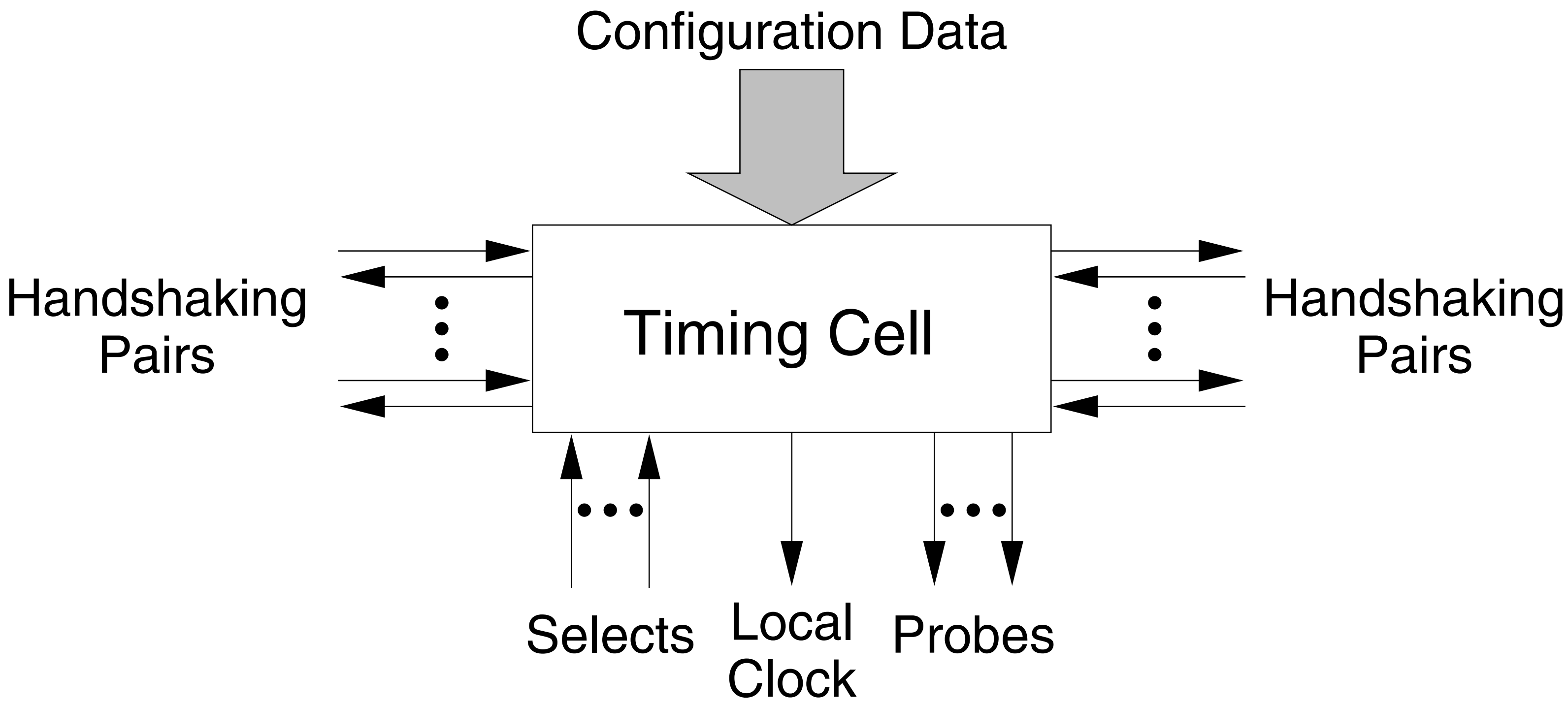


Toggled Branch

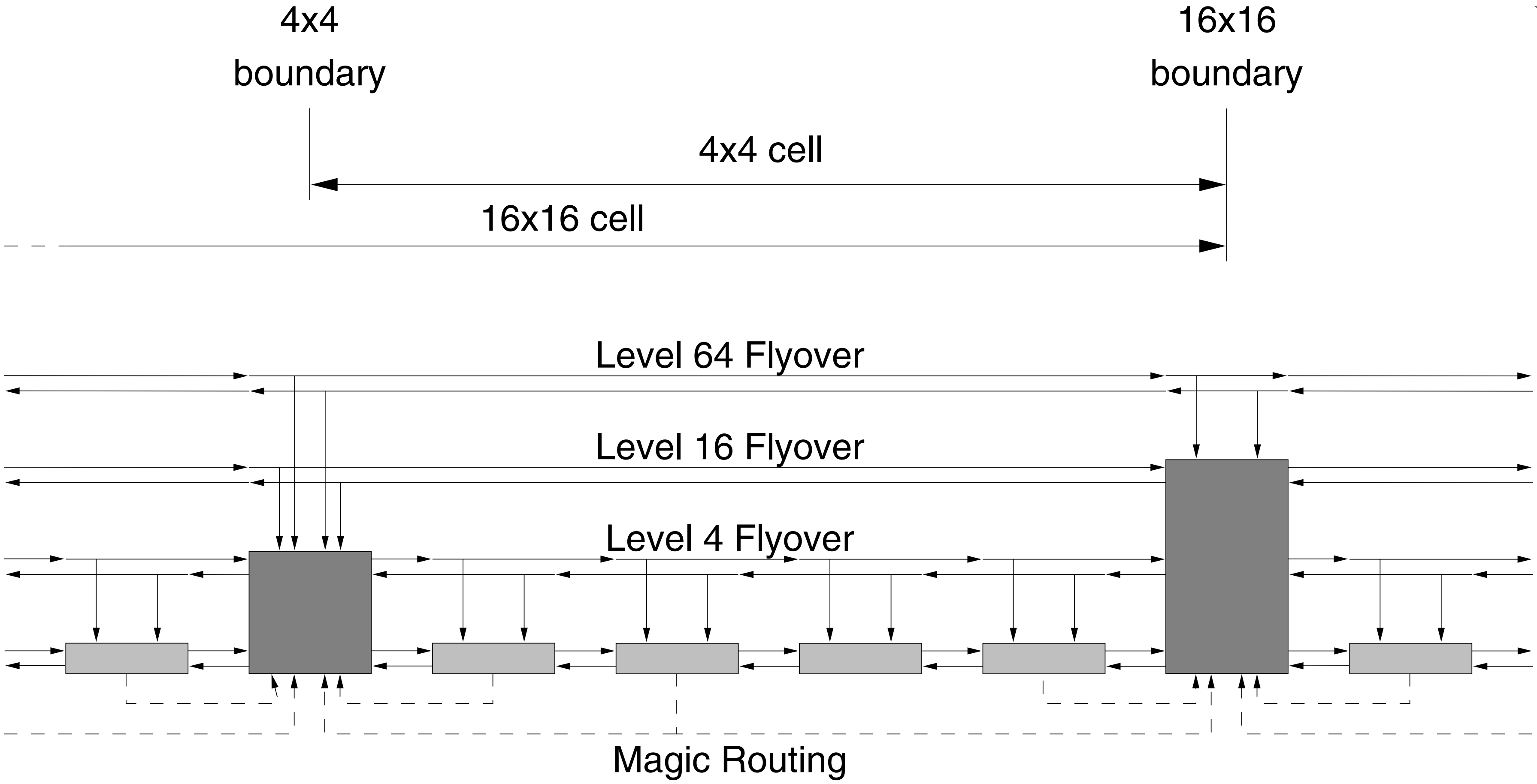


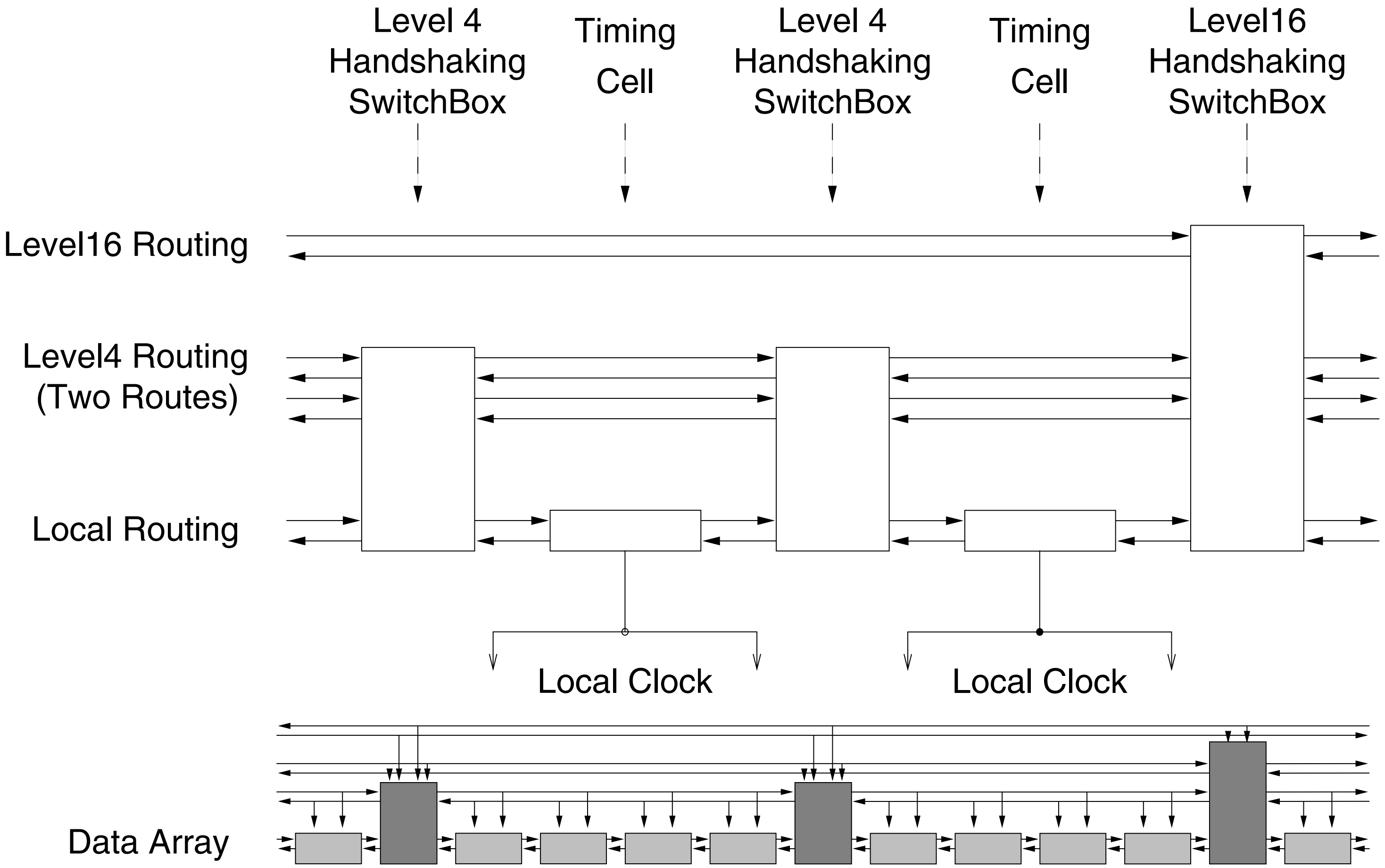


- Similar to Sutherland's Toggle, except operates on Handshaking Pairs



- Timing cell integrates synchronisation, control and delay elements
- Delay Elements: Reconfigurable Fixed Delay or CSCD


4x4
boundary
16x16
boundary
4x4 cell
16x16 cell
Level 64 Flyover
Level 16 Flyover
Level 4 Flyover
Magic Routing


Level 4
Handshaking
SwitchBox
Timing
Cell
Level 4
Handshaking
SwitchBox
Timing
Cell
Level16
Handshaking
SwitchBox
Level16 Routing
Level4 Routing
(Two Routes)
Local Routing
Local Clock
Local Clock
Data Array

Summary

- Reconfigurable Elements:
  - Reconfigurable C-Muller Gates
  - rC-Muller Cross-Bars : Routing
  - Select / Q-Merge Pair: Symmetry
- STACC Architecture Model
  - Timing cell integrates synchronisation, control and delay
  - Timing array has applicability beyond FPGAs.
- Self-Timed Xilinx XC6200 Architecture
  - See forthcoming PhD Thesis...