Dynamically Reconfigurable FPGAs

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What this talk is about:

- Basics of an FPGA architecture
- Configurable function blocks and interconnect
- Configuration memory
- Novel features of the Xilinx XC6200 FPGA
- Comments on some other topical FPGAs
- Issues raised by dynamic reconfiguration

A little history

FPGAs are successors to earlier forms of programmable logic:

- Programmable Logic Array (PLA)
- Programmable Array Logic (PAL)

Move from small number of gate equivalents to larger number (10,000–100,000).

Earlier devices:

- two-level logic function: boolean sum of products
- so, two planes: AND plane and OR plane

FPGAs use multi-level logic:

- Based on Mask Programmable Gate Arrays (MPGAs) — semi-custom implementation style for ASICs

Basic FPGA architecture

Basic components of an FPGA architecture:

- Configurable function blocks
- Configurable switchboxes and local interconnect
- Non-local interconnect
- Configuration memory

Further details:

- Function blocks arranged in regular two-dimensional array — possibly symmetrical, possibly hierarchical
- Switchboxes connect function inputs/outputs to interconnect
- Input/output switchboxes on array perimeter
- Contents of configuration memory determine the configurable aspects

Configurable function blocks

Functions:

- wide variety, but typically: boolean function of between 2–5 variables
- sometimes: latch or flip-flop as well

Basic styles:

- primitive gates (e.g., NAND or NOR)
- lookup tables (LUTs)
- multiplexors
- programmable array logic (PALs)

Often extras, such as:

- dedicated carry logic for adders
- memory structures

Configurable interconnect

Basic interconnection elements:

- bidirectional
- unidirectional
- open collector and tristate

Routing networks:

- separate routing channels with switchboxes at intersections
- routing integrated with function blocks (e.g., nearest neighbour)
- hybrids of the above, including hierarchies

Also:

- low-skew global clock signal routing

Configuration memory

Basic types:

- fuse-based: more compact, but externally programmed
- SRAM-based: configuration alterable within system

Configuration using SRAM-based approach:

- serially: provide all configuration data in sequence
- random access: addressable configuration memory

Random access SRAM is the approach needed for genuine dynamically reconfigurable FPGAs

Novel features of the Xilinx XC6200

The XC6200 is a random-access SRAM-based device:

- fine-grain function blocks: two-input logic function or multiplexor, plus flip-flop
- nearest-neighbour and hierarchical interconnect

Noteworthy features include:

- partial reconfiguration possible
- 'wildcard' configuration possible
- direct processor read/write access to registers configured on the array
- chip control signals can be driven from the array itself

A further plus is that the format of configuration data has been made freely available.

(Random) Other features of other FPGAs (I)

Xilinx XC4000:

- each block contains two 4-input LUTs and a 3-input LUT, plus two flip-flops - blocks can be configured as RAM
- support for carry chains
- variety of interconnect, including global nets

Altera Flex 10K (PLD):

- each block contains one 4-input LUT and one flip-flop
- blocks arranged in eight-high columns; support for carries
- array also has memory elements for RAM or for big LUTs

(Random) Other features of other FPGAs (II)

Atmel AT40K:

- each block contains two 3-input LUTs and one flip-flop
- nearest-neighbour connections to eight neighbours
- has dual-ported RAM elements

Issues for Research

Hard v. Soft:

- circuitry is soft, encoded in memory like programs
- conventional circuit design is predicated on the slow production of hardware
- conventional circuit interfacing is predicated on pins and wiring

FPGAs as system components:

- discrete FPGAs have narrow interfaces to processors or memory
- to use configurable logic well, need integration of logic, processor and memory components

Wide variety of styles:

- granularity of function blocks
- types of interconnection resource