UNIVERSITY OF EDINBURGH

FACULTY OF SCIENCE AND ENGINEERING

MASTER OF SCIENCE IN COMPUTER SCIENCE

CIRCUIT TECHNOLOGY FOR SYSTEM LEVEL INTEGRATION

Wednesday 26 April 2000

2:00 to 3:30

Examiners:

I. Watson (External)

R.N. Ibbett (Chairman)

INSTRUCTIONS TO CANDIDATES

Answer any TWO questions.

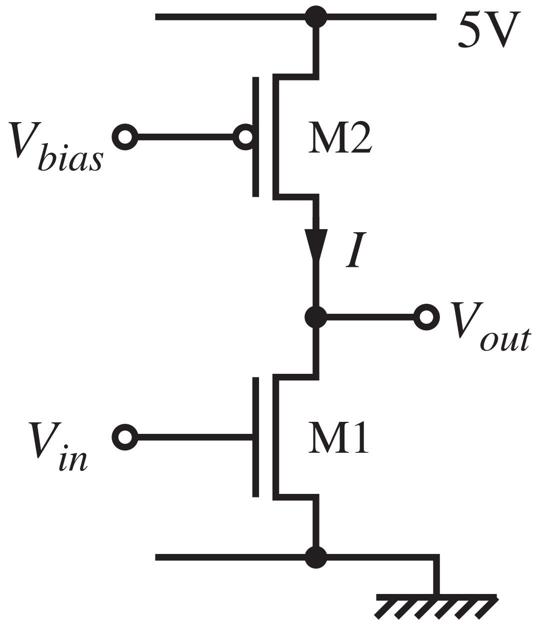
All questions carry equal weight.

1. (a) Show that the small-signal transconductance and drain resistance of a MOSFET working in the saturation region are given, approximately, by:
$g_m = \sqrt{2\beta I_{DS}}$ and $g_{DS} = \lambda I_{DS}$ respectively.

(6 marks)

(b) Find the current, I, and the value of V_{in} for the circuit shown below, given that V_{out} is to be 3V and that $V_{bias} = 4$V. The relevant process parameters and device dimensions are:-

$(W/L)_1 = 10\mu m/5\mu m$	$(W/L)_2 = 25\mu m/5\mu m$
$K_N = 35\mu A/V^2$	$K_P = 14\mu A/V^2$
$\lambda_N = 0.01$	$\lambda_P = 0.01$
$V_{TN} = 0.7$ V	$V_{TP} = -0.7$ V



CMOS amplifier with current-source load

(6 marks)

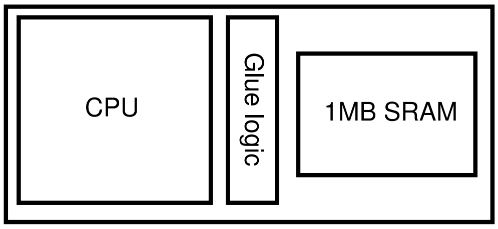
(c) Draw the small-signal model for the circuit shown above and find the circuit small-signal gain and output resistance.

(7 marks)

(d) Now use the value for I you calculated in (b), above, [or take $I = 5\mu$A if you could not attempt (b)] and find values for the small-signal gain and output resistance of the circuit.

(6 marks)

2. (a) A new chip is to be designed. This chip will comprise of 3 separate modules, SRAM, CPU and glue logic. The SRAM module will contain 0.5MB of memory. A similar 0.25 MB SRAM is manufactured in the same fabrication plant and has a yield of 80%. The CPU is not manufactured in the same plant but in an older sister plant and has a yield of 70%. The sister fabrication plant's yields are about 10% less than the the new plant. The glue logic has not yet been designed but will take approximately 10–15% of the CPU area and will have a similar critical area to the CPU.



Using the Poisson yield model,

$$Y = \prod_{i=1}^{N} e^{-\lambda_i}$$

estimate the chip yield. Give an estimate of the maximum and the minimum expected yield.

(13 marks)

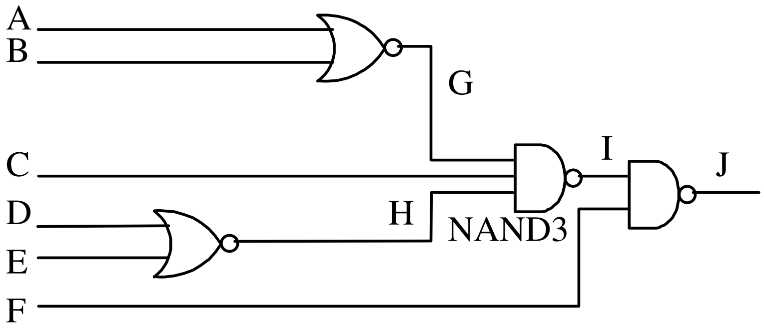
question continues overleaf

(b) Explain in no more than 40 words the difference between exhaustive, functional and structural test in a digital VLSI system

(4 marks)

(c) Describe in no more than 50 words the method of test-pattern generation based upon "single stuck-at" faults.

(4 marks)



CMOS amplifier with current-source load

(d) The above figure shows a small digital circuit. Develop a test pattern for a stuck-at-1 fault on node H.

(4 marks)

3. (a) What is the purpose of the technique known as ion implantation in the manufacture of integrated circuits. Describe briefly how ion implantation is achieved.

(3 marks)

(b) For each of the implants below used in a standard CMOS process give the dose and energy used and a brief description of the purpose of the implant, using diagrams where appropriate.

i. Field implant (channel stop implant).
ii. Threshold adjustment implant.
iii. Source/Drain implant.

(9 marks)

(c) Describe and relate the following terms as applied to a semi conductor "resistivity", "carrier mobility" and "sheet resistance"

(6 marks)

(d) Discuss the electrical and other (e.g. mechanical) properties of silicon and its compounds which make it a good candidate for semiconductor devices.

(7 marks)