UNIVERSITY OF EDINBURGH

FACULTY OF SCIENCE AND ENGINEERING

COMPUTER SCIENCE THREE

COMPUTER DESIGN

Friday 26 May 2000

11:30 to 13:00

Examiners:

Prof. K. Turner (External)

Prof. G. Brebner (Chairman)

INSTRUCTIONS TO CANDIDATES

Answer any TWO questions.

All questions carry equal weight.

1. A memory bus is to be shared between two devices which can act as bus masters, and a circuit is required which will arbitrate mastership of the bus between them. Each device provides a *bus request* (**BR**) signal to the arbiter, and receives a *bus grant* (**BG**) signal from the arbiter.

   The request/grant protocol is as follows:

   (a) When it desires to become bus master, a device asserts **BR**.

   (b) Some time later, the arbiter asserts **BG** to the device; this indicates to the device that it is now bus master.

   (c) When the device is finished with the bus, it deasserts **BR**.

   (d) The arbiter will then deassert **BG** to the device, which must not reassert **BR** to request more bus time until after **BG** has deasserted.

   Design a circuit to perform the bus arbitration. The arbitration should be fair, and must ensure that a requesting device always gets the bus eventually, given that devices are not allowed to keep their **BR** line asserted for ever. You should show clearly how your design is derived, indicate all the logic circuitry required, and state any additional assumptions you make. What components would you recommend for the implementation of your design? [*25 marks*]

2. The instruction set of a typical microprocessor will include instructions for integer add and multiply, and floating-point add and multiply. Explain the hardware that could be used to implement each of these operations, highlighting in particular what features of the hardware enable the operations to be carried out as rapidly as possible. [*25 marks*]

3. Provide short answers to *three* of the following (all parts carry equal credit):

   (a) Give an example of a combinational logic circuit which could exhibit a *hazard*. Describe the circumstances in which the hazard might occur, and explain why. How could the circuit be modified to prevent the hazard?

   (b) Explain how it is possible, by storing additional bits with each word written to memory in a computer system, to correct single errors, and detect double errors which occur in a stored word.

   (c) Outline the main components of a microcoded processor control section, explaining their function.

   (d) The bus which connects a processor to memory or to I/O controllers may be *synchronous* or *asynchronous*. Explain the differences between these two types of bus.

[*25 marks*]