UNIVERSITY OF EDINBURGH

FACULTY OF SCIENCE AND ENGINEERING

COMPUTER SCIENCE FOUR

HARDWARE VIRTUAL COMPONENT DESIGN

Monday 1 May 2000

09:30 to 11:00

Examiners:

Prof. K. Turner (External)

Prof. G. Brebner (Chairman)

INSTRUCTIONS TO CANDIDATES

Answer any TWO questions.

All questions carry equal weight.

1. (a) What is the distinction between *structural*, *behavioural* and *dataflow* modelling in VHDL? Describe a top-down approach to design development in VHDL which successively uses behavioural and structural descriptions. Explain how *configuration* blocks in VHDL assist in this approach. [*7 marks*]

   (b) Write an *entity* description for a *full adder* in VHDL. Also write architectural bodies corresponding to this entity which demonstrate the three main styles of VHDL description, namely, *structural* (using two half adders and an or-gate), *dataflow* (using a gate-level description), and *behavioural* (using sequentially executed statements). [*8 marks*]

   (c) What are the *concurrent* elements of your descriptions from part (b)? How can timing and gate delay information be introduced into your models? How and why are *wait* statements and *sensitivity* lists used in behavioural descriptions? [*4 marks*]

   (d) What is the simulation model used by VHDL? What are *transactions*, *events* and *drivers*? What is meant by the term *delta time* and how can the need for it arise? [*6 marks*]

2. (a) Describe briefly what is meant by the following levels of simulation:

- device
- circuit
- timing
- switch
- gate
- register-transfer
- system

[*7 marks*]

(b) How are signals modelled in terms of *levels* and *strengths* for gate-level simulation? Give examples. What propagation delay models might be used in gate-level simulation? [*6 marks*]

(c) How would a circuit be partitioned in preparation for a switch-level simulation? Describe the basic phases of operation of a switch-level simulator. [*6 marks*]

(d) What is meant by *Static Timing Analysis*? Describe briefly how it operates. What are its potential benefits over other forms of simulation? [*6 marks*]

3. (a) Why is a latch inferred when the following Verilog module is synthesised?

```
module latch (out, in, enable, reset);
output out;
input in, enable, reset;
reg out;

  always @(in or enable or reset)
    if (~reset) out = 0;
    else if (enable) out = in;

endmodule
```

[*4 marks*]

(b) Outline the generic structure of a Verilog module which models a Finite State Machine (FSM) in an *explicit* style. What would be the Verilog structure of an FSM modelled in an *implicit* style and when could this be used? [*8 marks*]

(c) What is meant by the term *scheduling* in behavioural synthesis? Outline the operation of a generic *List Scheduling* algorithm which attempts to minimise overall latency under resource availability constraints. What is a typical priority scheme for the list which is involved? [*8 marks*]

(d) How can List Scheduling be applied to the problem of minimising resource usage under latency constraints? [*5 marks*]