UNIVERSITY OF EDINBURGH

FACULTY OF SCIENCE AND ENGINEERING

COMPUTER SCIENCE THREE

COMPUTER ARCHITECTURE

Saturday 2 June 2001

09:30 to 11:00

Examiners:

K. Turner (External)

G. Plotkin (Chairman)

INSTRUCTIONS TO CANDIDATES

Answer any TWO questions.

All questions carry equal weight.

1. (a) Cache misses can be classified according to the "3 Cs". Describe the 3 Cs and the situations in which each occurs. Discuss how these might be affected by increasing the block size within a fixed overall cache size. [*8 marks*]

   (b) A processor has a 128 block frame, 4-way set associative cache, with 64 bytes of data per block; it uses 32 bit addresses. With the help of simple diagrams, describe the structure of such an address as it relates to the cache. Describe the actions which will be performed in the cache during execution of a load which results in a cache hit. [*9 marks*]

   (c) Consider the following code fragment

```
for (i=0; i<10000; i++)
   a[i] = a[i+1] + 2;
for (i=0; i<10000; i++)
   a[i] = a[i] - 3;
```

   Explain the concept of *loop fusion* and discuss how it can be applied in this situation. [*8 marks*]

2. (a) Describe the structure of the five stage DLX pipeline as examined during the course. You should explain the functions of each stage and their connectivity. [*8 marks*]

   (b) i. Define the term "Read-after-Write hazard" (RAW) and explain its significance for the DLX pipeline. [*4 marks*]

   ii. Consider the following instruction sequence (remembering that in DLX instructions the first operand is the destination):

```
LW   R1, 4(R2)
ADD  R2, R3, R4
SUB  R1, R3, R2
AND  R3, R1, R4
```

   Explain the RAW hazards which arise and describe which of these could be overcome with additional hardware. [*7 marks*]

   (c) Explain why the simple DLX pipeline is not vulnerable to "Write-after-Read" (WAR) hazards and discuss whether this is a strength or a weakness. [*6 marks*]

3. (a) Explain why successful branch prediction is crucial for modern high performance processors. [*6 marks*]

   (b) Static schemes use benchmark suites such as those maintained by SPEC to predict branch outcome. Suggest an advantage and a disadvantage of such approaches. [*4 marks*]

   (c) With the help of a simple program fragment explain why a typical branch prediction buffer would use two bits of prediction state rather than one. [*7 marks*]

   (d) Describe the contents and structure of a (2,2)-correlating branch prediction buffer. [*8 marks*]