UNIVERSITY OF EDINBURGH

FACULTY OF SCIENCE AND ENGINEERING

COMPUTER SCIENCE THREE

COMPUTER DESIGN

Monday 11 June 2001

09:30 to 11:00

Examiners:

K. Turner (External)

G. Plotkin (Chairman)

INSTRUCTIONS TO CANDIDATES

Answer any TWO questions.

All questions carry equal weight.

1. (a) Give tables showing how the state entered after the next clock signal depends on the current state and the input(s) for each of: (i) a **D**-type flip-flop, (ii) a **JK**-type flip-flop, and (iii) a **T**-type flip-flop. [*5 marks*]

(b) An **EPLD** contains eight JK-type flip-flops, all clocked from the same single clock input pin. The output of each flip-flop is available on a pin of the EPLD, and is also fed back internally into the EPLD AND-array. In addition, twelve input pins also feed into the AND-array.

The AND-array consists of 64 AND gates, each independently programmable to form any AND function of any of the twelve inputs and eight fed-back outputs, or their inverses. The EPLD OR-array contains sixteen OR gates, the inputs of each of which may be programmably connected to up to four of the 64 AND-array outputs. Each AND-array output may be connected to one OR gate only. Each of the sixteen OR gates feeds one of the sixteen inputs (eight J inputs and eight K inputs) to the eight JK-type flip-flops.

The device is to be programmed to form a fully synchronous eight-bit, loadable, resettable counter. The counter is to have eleven inputs – eight data inputs for loading the counter, plus active-high *Load*, *Reset* and *Count* control inputs. The counter is also to have eight outputs, giving the current count.

If *Reset* is asserted, the counter should reset to zero. Otherwise, if *Load* is asserted, the counter should load the input data. Otherwise, if *Count* is asserted the counter should count up by one. If none of the *Reset*, *Load* or *Count* inputs is asserted, the counter should hold its current count.

Give minimized sum-of-products expressions showing the required programming of the AND-OR array. (*Hint:* Karnaugh maps are not required.) [*10 marks*]

(c) Outline how would you modify your answer to (b) if the EPLD contained eight T-type flip-flops instead of JK-type, with the T input of each flip-flop fed from an OR gate which may be programmably connected to up to eight of the 64 AND gates in the array? (You do not need to supply full Boolean expressions.)

Why are T or JK-type flip-flops more suitable for counter applications than D-type flip-flops? [*5 marks*]

(d) What problems might occur if the inputs were asynchronous? How might these problems be alleviated? [*5 marks*]

2. (a) Explain the distinction between the *control section* and the *data path* of a processor. [*5 marks*]

   (b) Taking a wide definition of a processor as 'a sequential system for processing data', discuss, with examples, how the complexity of the control section depends both on the complexity of the data path, and on the complexity of the operations the processor is to perform. [*20 marks*]

3. Provide short answers to *three* of the following (all parts carry equal credit):

   (a) What parts are required (i) in an I/O controller, and (ii) in the rest of the computer, to support I/O transfer by *direct memory access*?

   (b) A computer system usually contains many I/O subsystems able to interrupt the CPU. What software and hardware mechanisms might be used to identify the source of an interrupt?

   (c) A *SECDED* system allows single-bit errors occurring in a memory word to be corrected, and two-bit errors to be detected. Explain how this is done.

   (d) What are *tri-state* and *open-collector* (or *open-drain*) logic outputs, and why are they useful?

[*25 marks*]