UNIVERSITY OF EDINBURGH

FACULTY OF SCIENCE AND ENGINEERING

MASTER OF SCIENCE IN COMPUTER SCIENCE

CONCURRENT COMPUTER ARCHITECTURE

Thursday 26 April 2001

14:00 to 15:30

Examiners:

I. Watson (External)

R.N. Ibbett (Chairman)

INSTRUCTIONS TO CANDIDATES

Answer any TWO questions.

All questions carry equal weight.

1. (a) Describe a mechanism for implementing stacking/unstacking instructions in a computer with a one-address instruction format.

   With the aid of diagrams and/or code examples, show how these instructions can be used in

   i. the evaluation of complex expressions
   ii. procedure calling

   [*8 marks*]

   (b) Explain why computers with a three-address instruction format normally have one or more sets of addressable registers.

   Using any appropriate assembly code notation, write a sequence of instructions for such a computer which will execute the following high-level language program fragment:

```
b = 0;
for (i = 0; i < j; i++) {
   x [i] = y [i] - a;
   b = (b + x [i])/j;
}
```

   where x and y are arrays and a, b and j are scalar values, all held in store. State clearly what each instruction does. [*9 marks*]

   (c) Explain how a system of register windows works and show how these registers would be used in procedure calling.

   Compare and contrast this mechanism with the use of stacking instructions in part (a)(ii). [*8 marks*]

2. (a) Explain the principles of pipelining and derive a formula which shows the speed-up (S) obtained by pipelining as a function of k, the number of stages in the pipeline, and n, the number of data items being processed. [*5 marks*]

   (b) Explain the significance of the Control Point in a pipeline and state briefly the arguments for placing the Control Point

      i. early in the pipeline
      ii. late in the pipeline

   [*6 marks*]

   (c) Explain the principles of operation of a Branch Target Address Cache (BTAC) and show how it attempts to overcome the effects of branches on pipeline performance. [*6 marks*]

   (d) Measurements taken from a certain pipelined processor with a BTAC show that for a particular benchmark program, 4% of the instructions executed are unconditional branches and 8% conditional branches of which 80% actually cause a control transfer. Conditional branches incur an average penalty of 2 clock periods waiting for their condition to be evaluated and all incorrectly predicted branches incur a 6 clock penalty. All other instructions take, on average, 1.5 clocks to execute. The BTAC correctly predicts 80% of the unconditional and 75% of the conditional instructions. Calculate the average number of clocks per instruction when this benchmark is run:

      i. with the BTAC turned on
      ii. with the BTAC turned off

   [*8 marks*]

3. (a) Explain what is meant by *virtual memory* and with the aid of diagrams explain the role of Current Page Registers in its implementation. [*5 marks*]

   (b) With the aid of diagrams, explain the distinction between *shared memory* and *message passing* systems of multiple processors. Show how values are passed between processors in each type of system. [*6 marks*]

   (c) Explain the distinction between shared memory systems which offer:

      i. uniform memory access time
      ii. non-uniform memory access time

   In each case draw a block diagram of a typical system. [*6 marks*]

   (d) Briefly discuss the advantages and disadvantages of hypercubes and 3D meshes as multiprocessor interconnection networks in terms of their scalability with respect to

      i. network diameter
      ii. node degree
      iii. network throughput $\left(\propto \frac{\textit{number of connections}}{\textit{average message distance}}\right)$

   Give values for these parameters for a 512 processor system built using each type of network. [*8 marks*]