UNIVERSITY OF EDINBURGH

FACULTY OF SCIENCE AND ENGINEERING

MASTER OF SCIENCE IN COMPUTER SCIENCE

HARDWARE VIRTUAL COMPONENT DESIGN

Tuesday 24 April 2001

14:00 to 15:30

Examiners:

I. Watson (External)

R.N. Ibbett (Chairman)

INSTRUCTIONS TO CANDIDATES

Answer any TWO questions.

All questions carry equal weight.

1. (a) What is meant by the *Standard Cells* style of circuit layout? What kind of cells are typically part of a Standard Cells library and how are they designed? How are the cells interconnected in a layout? [*5 marks*]

   (b) What criteria might be taken into account when deciding on the placement of individual cells in a Standard Cells layout and what is the significance of each criterion? [*6 marks*]

   (c) Briefly describe the semi-perimeter technique of wirelength estimation used during placement optimisation. What other techniques might be considered and why? [*6 marks*]

   (d) Distinguish between *constructive* and *iterative improvement* methods of cell placement. Describe how techniques of *simulated annealing* can be used in an iterative improvement placement method. What types of perturbation of each configuration could be used and what might a suitable cost function involve? [*8 marks*]

2. (a) What is meant by the terms *structural* and *behavioural* modelling in Hardware Description Languages? Compare the structural modelling capabilities of VHDL and the Model language. [*6 marks*]

   (b) What is the timing model used in VHDL descriptions and how does this relate to its event-based simulation model? [*6 marks*]

   (c) How are *behavioural* descriptions written in VHDL? Explain the function of process *sensitivity* lists and *wait* statements. [*6 marks*]

   (d) Outline how a Finite State Machine could be modelled behaviourally in VHDL. Exemplify your answer with either the controller for a simple traffic lights system or any other simple system. [*7 marks*]

3. (a) List the typical stages in a behavioural synthesis system, briefly describing the function of each. [*6 marks*]

(b) Outline algorithms which create As-Soon-As-Possible (ASAP) and As-Late-As-Possible (ALAP) schedules. [*6 marks*]

(c) Draw a sequencing graph for the following expression:

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(a-b)*(c-d)*(e-f)*(g-h)
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Convert this (*i*) to an ASAP schedule and (*ii*) to an ALAP schedule. How much *slack* is present? [*7 marks*]

(d) How can the following *timing constraints* be represented on a sequencing graph?

i. a *minimum* time between two operations

ii. a *maximum* time between two operations

What is the criterion which determines the existence of a consistent schedule in the case of the maximum timing constraint? [*6 marks*]