UNIVERSITY OF EDINBURGH

FACULTY OF SCIENCE AND ENGINEERING

COMPUTER SCIENCE THREE

COMPUTER DESIGN

Tuesday 11 June 2002

14:00 to 15:30

Examiners:

Prof. K. Turner (External)

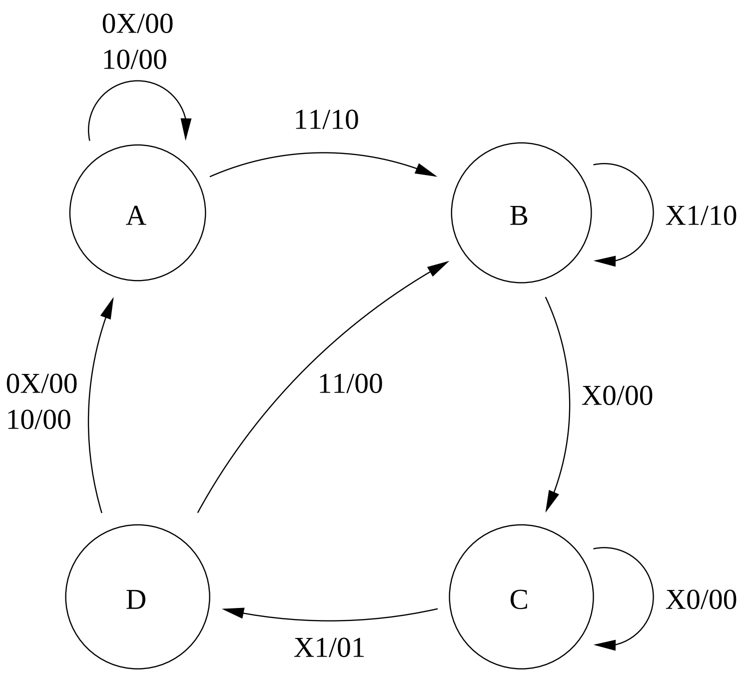
Prof. C. Stirling (Chairman)

INSTRUCTIONS TO CANDIDATES

Answer any TWO questions.

All questions carry equal weight.

1. (a) A circuit is required, with two inputs, `X` and `Y`, and two outputs, `Q` and `R`, which will operate as defined by the following state diagram. (Transitions in the diagram are labelled in the format `XY/QR`.)



Design a synchronous sequential logic circuit to perform this function. You should show all the steps in the derivation of your design, and should provide circuit diagrams for your design, using only NAND gates, inverters and flip-flops. [*13 marks*]

(b) Describe *two* ways you could modify your design to ensure that the circuit starts in the state labelled A when powered up. [*4 marks*]

(c) How would you decide a suitable clock speed for your circuit? [*2 marks*]

(d) Explain how your circuit might malfunction if the inputs are asynchronous to the clock. How would you fix this problem? Would your solution completely prevent the malfunction, and why? [*6 marks*]

2. (a) Draw a block diagram of a datapath suitable for a simple non-pipelined microprocessor, at a level of detail showing registers and principal data-processing block(s). Explain the function of each part of the datapath, and outline the signals by which each part would be controlled. [*9 marks*]

   (b) Show how your datapath would be used to implement one example of each of the following categories of instruction: load register from memory, store register to memory, arithmetic on registers, conditional branch. [*10 marks*]

   (c) Draw a Mealy machine state diagram for a control section which would implement your four example instructions, on your datapath. Your diagram should clearly show the input conditions, and asserted outputs, associated with each state transition. [*6 marks*]

3. Provide short answers to *three* of the following (all parts carry equal credit):

   (a) What is a *carry-save adder*? Show how a number of carry-save adders and a single look-ahead carry adder can be used to implement a fast, fully combinational circuit for multiplying two unsigned 4-bit numbers. Estimate the maximum propagation delay of the circuit, in terms of gate delays.

   (b) By referring to the bit storage cell circuit structure in each device, explain the differences in volatility of data stored in a static RAM device, a dynamic RAM device and an EPROM device.

   (c) Describe the operations involved in, and the hardware features required for, loading and storing of 8-bit and 16-bit operands between a CPU register and a 32-bit wide memory system. What is meant by *little-* and *big-endian*?

   (d) Outline the differences between *synchronous* and *asynchronous* sequential logic circuits. Why are the former usually easier to design?

[*25 marks*]