UNIVERSITY OF EDINBURGH

FACULTY OF SCIENCE AND ENGINEERING

COMPUTER SCIENCE THREE

COMPUTER ARCHITECTURE

Tuesday 5 September 2000

14:00 to 15:30

Examiners:

K. Turner (External)

G. Brebner (Chairman)

INSTRUCTIONS TO CANDIDATES

Answer any TWO questions.

All questions carry equal weight.

1. (a) Sketch the structure of Hennessy and Paterson's DLX RISC pipeline and explain the work carried out at each stage. [*7 marks*]

   (b) Consider the following DLX loop

```
loop: LW    R1, 0(R2)
      ADDI  R1, R1, #1
      SW    0(R2), R1
      ADDI  R2, R2, #4
      SUB   R4, R3, R2
      BNEZ  R4, loop
```

   For each of the techniques listed below, explain the principle involved and discuss whether it could improve pipeline performance when executing the loop.

   i. split cycle register access
   ii. forwarding
   iii. delayed branching [*12 marks*]

   (c) With the help of a small fragment of C code, explain the difference between **non-correlating** and **correlating** branch prediction techniques. [*6 marks*]

2. (a) Architecture X has a **direct mapped cache** and uses 32 bit addresses consisting of 19 bits of tag, 8 bits of index and 5 bits of offset.

   i. Sketch the structure of such a direct mapped cache, indicating how the various address bits are used to access data.

   ii. Explain how much can deduced about the size of X's cache. *[9 marks]*

   (b) Explain the concept and structure of a **victim cache**, discussing the circumstances under which it can be expected to improve the performance of the memory hierarchy. *[8 marks]*

   (c) With the help of short fragments of C code, explain the purpose of the compiler optimisations known as

   i. loop fusion

   ii. loop interchange *[8 marks]*

3. (a) Derive Amdahl's law and explain its significance for computer architects. [*8 marks*]

(b) Vector Processors (VPs) were popular during the late 20th century because of their suitability for executing programs involving regular operations on arrays. The typical VP had two modes of execution, a conventional "scalar mode" and a special array-oriented "vector mode" for fast processing of array operations which would normally be handled by loops. The overall speed-up for a computation on a VP is defined as the ratio of the run time for executing the whole computation in scalar mode to the run time when vector mode is used for some part of the execution.

Explain the application of Amdahl's Law to Vector Processors and sketch the shape of the curve which would be observed by plotting overall speed up against percentage of a computation which uses vector mode for a machine with a vector mode which is 30 times faster than the equivalent computation in scalar mode. [*7 marks*]

(c) Deduce the fraction of a computation which must execute in vector mode to achieve an overall speed-up of 3, for the machine of part (b). [*4 marks*]

(d) With reference to your sketch from (b), discuss the merits of putting effort into

i. the compiler, with a view to increasing the percentage of code which uses vector mode

ii. reducing the clock speed (equally in both modes) [*6 marks*]